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Application No: 10/761,343
Attorney's Docket No: ALC 3113**CLAIM AMENDMENTS**

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims

1. (Previously Presented) A printed wiring board (PWB) for mounting a high performance ball grid array (BGA) device on one side of said PWB, comprising:

a modified vias array, the modification being that at least a portion of one column of said vias array is missing at least two adjacent vias, wherein the missing vias have been replaced by respective shared vias in an adjacent row, and said shared vias have been connected to either a power supply or a power return; and

a via pad for each said shared vias located on the other side of said PWB in said portion, whereby a decoupling capacitor can be electrically connected across said pair of via pads to decouple the power supply and the power return at said two adjacent vias.

2. (Currently Amended) A printed wiring board (PWB) for mounting a high performance integrated circuit, comprising:

on a top side of said PWB, a modified via array with BGA columns and BGA rows of ball connection pads;

a modified vias array of plated through hole (PTH) vias, with each via column Col(n) arranged between two respective BGA columns c(n) and c(n+1) and each via row R(k) arranged between two respective BGA rows r(k) and r(k-1),

Application No: 10/761,343
 Attorney's Docket No: ALC 3113

wherein $2m$ vias of said via column $Col(i)$ placed in successive via rows ~~$R(i)$~~ rows $R(j)$ to $R(j+2m-1)$ of said modified vias array are depopulated to obtain a free space on the back side of said PWB,

wherein $2m$ corresponding vias in a via column $Col(i+1)$ adjacent to said via column $Col(i)$ and placed in said successive via rows $R(j)$ to $R(j+2m-1)$ of said vias array are shared vias, and

wherein $n \geq 1$, $k \geq 2$, $j \geq 2$, $k \geq 2$, $2 \leq i < n$ and $j < k$.

3. (Original) The PWB of claim 2, wherein said free space has a width $D1$ equal to twice the pitch D of said vias array less a via size, for accommodating m passive elements of a substantially similar width $D1$.
4. (Original) The PWB of claim 2, wherein m is at least one.
5. (Currently Amended) The PWB of claim 2, wherein a first shared via in said via column ~~$Col(i)$~~ column $Col(i+1)$ and said via row $R(j)$ provides a power contact to a first associated ball contact pad in said via column ~~$c(i)$~~ column $c(i+1)$ and said via row $r(j)$ and to a second associated ball contact pad in said via column ~~$c(i+1)$~~ column $c(i+2)$ and said via row $r(j)$.
6. (Currently Amended) The PWB of claim 5, wherein a second shared via in said via column ~~$Col(i)$~~ column $Col(i+1)$ and said via row $R(j+1)$ provides a ground contact to a third

Application No: 10/761,343
Attorney's Docket No: ALC 3113

associated ball contact pad in said via ~~column c(i)~~column c(i+1) and said via row r(j+1) and to a fourth associated ball contact pad in said via ~~column c(i+1)~~column c(i+2) and said via row r(j).

7-8. (Cancelled)

9. (Previously Presented) The PWB of claim 2, wherein a first shared via in said via column Col(i) and said via row R(j) provides a power contact to a first associated ball contact pad in said via column c(i) and said via row r(j+1) and to a second associated ball contact pad in said via column c(i+1) and said via row r(j).

10. (Previously Presented) The PWB of claim 9, wherein a second shared via in said via column Col(i) and said via row R(j+1) provides a ground contact to a third associated ball contact pad in said c(i) and said via row r(j+2) and to a fourth associated ball contact pad in said via column c(i+1) and a via row r(j+1).

11. (Original) The PWB of claim 3, wherein said passive elements are 0603, 0402, 0201 or smaller decoupling capacitors.

12. (Original) The PWB of claim 3, wherein said passive elements are 0603, 0402, 0201 or smaller resistors.

Application No: 10/761,343
Attorney's Docket No: ALC 3113

13. (Withdrawn) For a printed wiring board (PWB) having a land pattern for mounting a BGA device on one side of said PWB and a vias array for connecting said BGA device to said PWB a method for mounting a decoupling capacitor on the other side of said PWB, comprising:
- depopulating at least two adjacent vias in a portion of a first row of said vias array;
 - replacing said depopulated vias by a pair of shared vias in a second row, adjacent to said first row;
 - connecting said shared vias to a power supply and a power return respectively and providing a respective via pad for said shared vias on the other side of said PWB in said portion;
 - and
 - electrically connecting said decoupling capacitor across said pair of shared vias to decouple the power supply and the power return at said two adjacent vias.